



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/660,190

09/11/2003

Eric D. Groen

X-1420 US

5845

24309

7590

11/08/2006

XILINX, INC

ATTN: LEGAL DEPARTMENT

2100 LOGIC DR

SAN JOSE, CA 95124

EXAMINER

FILE, ERIN M

ART UNIT

PAPER NUMBER

2611

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

ST

| | | | |
|------------------------------|--------------------------------------|---------------------------------------|--|
| Office Action Summary | Application No. 10/660,190 | Applicant(s) GROEN, ERIC D. | |
| | Examiner Erin M. File | Art Unit 2611 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 19-23 is/are allowed.
- 6) ☒ Claim(s) 1-6, 15-17 is/are rejected.
- 7) ☒ Claim(s) 7-14 and 18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- 1. ☐ Certified copies of the priority documents have been received.
 - 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>1/16/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutkemeyer (U.S. Pub. No. 2001/0049812) in view of Nascimento (U.S. Pub. No. 2005/0024103) and Tomlinson et al. (U.S. Pub. No. 2002/0104031).

Claim 1, Lutkemeyer discloses a multi-giga bit transceiver (MGT, abstract, lines 1-3) including:

- first MGT circuitry for performing a first MGT function (fig. 1, 30, circuit A performing a first function);
- second MGT circuitry for performing a second MGT function (fig. 1, 32, circuit B performing a second function);

Lutkemeyer fails to disclose:

- at least one regulated power source and at least one unregulated power source, both coupled to selectively provide regulated and unregulated power to the first and second MGT circuitry;

Art Unit: 2611

- programmable logic for providing control signals to select and operatively couple the first and second MGT circuitry to one of the at least one regulated and unregulated power sources.

However, Nascimento discloses:

- at least one regulated power source and at least one unregulated power source, both coupled to selectively provide regulated and unregulated power to the first and second MGT circuitry (abstract, lines 5-11);

As Nascimento discloses that his invention keeps power losses very low ([0017], lines 5-7) it would be obvious to one skilled in the art at the time of invention to incorporate the power sources as disclosed by Nascimento into the invention of Lutkemeyer. Nascimento fails to disclose:

- programmable logic for providing control signals to select and operatively couple the first and second MGT circuitry to one of the at least one regulated and unregulated power sources.

However, Tomlinson discloses a switch programmable logic for providing control signals to select and operatively couple the first and second MGT circuitry to one of the at least one regulated and unregulated power sources (abstract).

Because programmable power management allows for more efficient use power in a circuit, it would have been obvious to one skilled in the art at the time of invention to incorporate the power switching and regulation as disclosed by Tomlinson into the combined invention of Lutkemeyer and Nascimento.

Claim 2, Nascimento further discloses at least one regulated power source comprises an unregulated supply and a plurality of power regulators (abstract,

Art Unit: 2611

lines 5, 8-9, first and second power regulators are disclosed) and Tomlinson discloses selective coupling of power from the supply to the first and second circuitry (abstract).

3. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lutkemeyer (U.S. Pub. No. 2001/0049812), Nascimento (U.S. Pub. No. 2005/0024103), and Tomlinson et al. (U.S. Pub. No. 2002/0104031) as applied to claims 1, 2 above, and further in view of Liu (U.S. Pub. No. 2005/0169416).

Claims 3-5, although neither Lutkemeyer, Nascimento, nor Tomlinson discloses the first MGT circuitry comprises a phase-locked loop (PLL), Liu discloses a transceiver which uses a phase lock loop which provides timing for the transmitting and receiving functions of the transceiver ([0006]). Because phase locked loops are well known in the art for the advantage of providing synchronized clocks in a transmitter or receiver, it would have been obvious to one skilled in the art at the time of invention to incorporate the phase locked loops as disclosed by Liu into the combined invention of Lutkemeyer, Nascimento, and Tomlinson.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lutkemeyer (U.S. Pub. No. 2001/0049812), Nascimento (U.S. Pub. No. 2005/0024103), Tomlinson et al. (U.S. Pub. No. 2002/0104031), and Liu (U.S. Pub. No. 2005/0169416) as applied to claim 5 above, and further in view of Agarwal et al. (U.S. Pub. No. 2004/0212394).

Art Unit: 2611

Claim 6, Lutkemeyer, Nascimento, Tomlinson, and Liu fail to disclose a serial-in-parallel-out circuitry, Agarwal discloses a receiver serial-in-parallel-out circuitry (Rx SIPO) [0031]. The use of a serial-in-parallel-out circuitry allows for faster data processing at the receiver end and would therefore be obvious to one skilled in the art at the time of invention to incorporate the serial-in-parallel-out as disclosed by Agarwal into the combined invention of Lutkemeyer, Nascimento, Tomlinson, and Liu.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khamis et al. (U.S. Patent No. 5,930,729) in view of Brambilla et al. (U.S. Patent No. 6,072,359) and Beck (U.S. Pub. No. 2001/0020842).

Claim 15, Khamis discloses:

- a voltage regulator with an output node coupled a selectable switch to selectively provide regulated power to at least one of a transmit PLL (col. 14, lines 38-41)

Khamis fails to disclose:

- a current mirror having a reference current stage and selectable current mirror stages for providing one of a plurality of current levels into an output node

However, Brambilla discloses:

- a current mirror having a reference current stage and selectable current mirror stages for providing one of a plurality of current levels into an output node (col. 13, lines 53, col. 13, line 63 – col. 14, line 2)

Art Unit: 2611

Brambilla discloses that current mirror circuits in voltage regulators have the advantage of having excellent response speeds, even at high frequencies (col. 2, lines 51-56). Because of this advantage it would have been obvious to one skilled in the art at the time of invention to incorporate the current mirror circuit as disclosed by Brambilla into the invention of Khamis. Neither Khamis nor Brambilla disclose:

- a voltage regulator stage coupled to adjustably sink current from and source current to the output node to maintain a specified output voltage at the output node

However, Beck discloses:

- a voltage regulator stage coupled to adjustably sink current from and source current to the output node to maintain a specified output voltage at the output node (abstract)

Beck further discloses that this type of voltage regulation has the advantage of providing self-configurability in a transceiver environment ([011], lines 15-17).

Because of this advantage it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage regulator with current sink and source as disclosed by Beck into the combined invention of into the invention of Khamis and Brambilla.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khamis et al. (U.S. Patent No. 5,930,729), Brambilla et al. (U.S. Patent No.

Art Unit: 2611

6,072,359), and Beck (U.S. Pub. No. 2001/0020842) as applied to claim 15 above, and further in view of Agarwal et al. (U.S. Pub. No. 2004/0212394).

Claim 16, Khamis discloses a selectively coupled output. Neither Khamis, Brambilla, nor Beck discloses a serial-in-parallel-out circuitry, Agarwal discloses a receiver serial-in-parallel-out circuitry (Rx SIPO) [0031]. The use of a serial-in-parallel-out circuitry allows for faster data processing at the receiver end and would therefore be obvious to one skilled in the art at the time of invention to incorporate the serial-in-parallel-out as disclosed by Agarwal into the combined invention of Khamis, Brambilla, and Beck.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khamis et al. (U.S. Patent No. 5,930,729), Brambilla et al. (U.S. Patent No. 6,072,359), and Beck (U.S. Pub. No. 2001/0020842) as applied to claim 15 above, and further in view of Bourke et al. (U.S. Patent No. 3,656,006).

Claim 17, Neither Khamis, Brambilla, nor Beck discloses the voltage regulator stage further includes an amplifier and a voltage divider with selectable divider resistors to create selectable voltage divider ratios, the voltage divider coupled to an input of the amplifier. However, Bourke discloses an amplifier and a voltage divider with selectable divider resistors to create selectable voltage divider ratios, the voltage divider coupled to an input of the amplifier (col. 4, lines 54-65). Selectable voltage divider ratios allow for more robust and flexible design and would therefore be obvious to one skilled in the art at the time of invention to

Art Unit: 2611

incorporate the voltage dividing as disclosed by Bourke into the combined invention of Khamis, Brambilla, and Beck.

Allowable Subject Matter

8. Claims 7-14, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 19-23 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter: The limitation of claim 19 regarding selecting between regulated power and unregulated power and generating corresponding control signals to circuitry for generating the transmitter and receiver clocks and circuitry for converting the parallel data into serial data is not found in the prior art of record.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2611

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Erin M. File

EMF

11/1/2006


MOHAMMED CHAYOUR
SUPERVISORY PATENT EXAMINER